Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1-15. (Canceled)

16. (Currently Amended) A method for forming an active matrix circuit comprising a transistor, said method comprising:

forming an active layer comprising a plurality of semiconductor islands arranged in parallel to each other over a substrate;

doping a p-type impurity into ~~a semiconductor~~ said active layer by ion doping to form a source region and a drain region in said ~~semiconductor~~ active layer, said ~~semiconductor~~ active layer comprising a part to become a channel region between said source region and said drain region;

forming a gate electrode adjacent to said part to become said channel region;

activating said p-type impurity by annealing; [[and]]

forming an interlayer insulating film comprising a silicon nitride layer and a silicon oxide layer over said ~~semiconductor~~ active layer by plasma CVD, said silicon nitride layer and said silicon oxide layer formed over said gate electrode and said ~~semiconductor~~ active layer; and

forming a conductive layer comprising titanium and aluminum over said interlayer insulating film,

wherein said transistor of said active matrix circuit comprises said channel region and said gate electrode and said source region and said drain region.

17. (Previously Presented) A method according to claim 16 wherein said active matrix circuit is incorporated into a liquid-crystal display.

18. (Previously Presented) A method according to claim 16 wherein said active matrix circuit is incorporated into an image sensor.

19. (Previously Presented) A method according to claim 16 wherein said active matrix circuit is incorporated into a liquid-crystal electro-optical device.

20. (Currently Amended) A method according to claim 16 wherein ~~said semiconductor layer comprises an amorphous semiconductor island having~~ each of said semiconductor islands comprises amorphous semiconductor and has a plane area of 1000 μm^2 or less.

21. (Currently Amended) A method according to claim 20 further comprising crystallizing said amorphous semiconductor ~~island~~.

22. (Currently Amended) A method for forming an active matrix circuit comprising a transistor, said method comprising:

forming an active layer comprising a plurality of semiconductor islands arranged in parallel to each other over a substrate;

doping a p-type impurity into ~~a semiconductor~~ said active layer by ion doping to form a p-type impurity region in said ~~semiconductor~~ active layer, said ~~semiconductor~~ active layer comprising a part to become a channel region adjacent to said p-type impurity region;

forming a gate electrode adjacent to said part to become said channel region;

activating said p-type impurity by annealing; [[and]]

forming an interlayer insulating film comprising a silicon nitride layer and a silicon oxide layer over said ~~semiconductor~~ active layer by plasma CVD, said silicon nitride layer and said silicon oxide layer formed over said gate electrode and said ~~semiconductor~~ active layer; and

forming a conductive multi-layer film comprising a titanium layer and an aluminum layer over said interlayer insulating film,

wherein said transistor of said active matrix circuit comprises said channel region and said gate electrode and said p-type impurity region.

23. (Previously Presented) A method according to claim 22 wherein said active matrix circuit is incorporated into a liquid-crystal display.

24. (Previously Presented) A method according to claim 22 wherein said active matrix circuit is incorporated into an image sensor.

25. (Previously Presented) A method according to claim 22 wherein said active matrix circuit is incorporated into a liquid-crystal electro-optical device.

26. (Currently Amended) A method according to claim 22 wherein ~~said semiconductor layer comprises an amorphous semiconductor island having~~ each of said semiconductor islands comprises amorphous semiconductor and has a plane area of 1000 μm^2 or less.

27. (Currently Amended) A method according to claim 26 further comprising crystallizing said amorphous semiconductor ~~island~~.

28. (Currently Amended) A method for forming an active matrix circuit comprising a transistor, said method comprising:

forming an active layer comprising a plurality of semiconductor islands arranged in parallel to each other over a substrate;

doping a p-type impurity into ~~a semiconductor~~ said active layer by ion doping to form a p-type impurity region in said ~~semiconductor~~ active layer, said ~~semiconductor~~ active layer comprising a part to become a channel region adjacent to said p-type impurity region;

forming a gate electrode adjacent to said part to become said channel region;

activating said p-type impurity by annealing;

forming an interlayer insulating film comprising a silicon nitride layer and a silicon oxide layer over said ~~semiconductor~~ active layer by plasma CVD, said silicon nitride layer and said silicon oxide layer formed over said gate electrode and said ~~semiconductor~~ active layer; and

forming a conductive layer comprising titanium and aluminum over said interlayer insulating film,

wherein said transistor of said active matrix circuit comprises said channel region and said gate electrode and said p-type impurity region.

29. (Previously Presented) A method according to claim 28 wherein said conductive layer comprises an electrode.

30. (Previously Presented) A method according to claim 28 wherein said conductive layer comprises a wiring.

31. (Previously Presented) A method according to claim 28 wherein said active matrix circuit is incorporated into a liquid-crystal display.

32. (Previously Presented) A method according to claim 28 wherein said active matrix circuit is incorporated into an image sensor.

33. (Previously Presented) A method according to claim 28 wherein said active matrix circuit is incorporated into a liquid-crystal electro-optical device.

34. (Currently Amended) A method according to claim 28 wherein ~~said semiconductor layer comprises an amorphous semiconductor island having~~ each of said semiconductor islands comprises amorphous semiconductor and has a plane area of 1000 μm^2 or less.

35. (Currently Amended) A method according to claim 34 further comprising crystallizing said amorphous semiconductor ~~island~~.

36. (Previously Presented) A method according to claim 28 wherein said conductive layer comprises a multi-layer film including a titanium layer and an aluminum layer.

37-45. (Canceled)

46. (Currently Amended) A method for forming an active matrix circuit comprising a transistor, said method comprising:

forming an active layer comprising a plurality of semiconductor islands arranged in parallel to each other over a substrate;

doping a p-type impurity into ~~a semiconductor~~ said active layer by ion doping to form a source region and a drain region in said ~~semiconductor~~ active layer, said ~~semiconductor~~ active layer comprising a part to become a channel region between said source region and said drain region;

forming a gate electrode adjacent to said part to become said channel region;

activating said p-type impurity by annealing; [[and]]

forming a first interlayer insulating film comprising a silicon nitride layer and a silicon oxide layer over said ~~semiconductor~~ active layer by plasma CVD, said silicon nitride layer and said silicon oxide layer formed over said gate electrode and said ~~semiconductor~~ active layer;

forming a conductive layer comprising a titanium and an aluminum over said first interlayer insulating film;

forming a second interlayer insulating film over said conductive layer; and

forming a pixel electrode over said second interlayer insulating film,

wherein said transistor of said active matrix circuit comprises said channel region and said gate electrode and said source region and said drain region.

47. (Previously Presented) A method according to claim 46 wherein said active matrix circuit is incorporated into a liquid crystal display.

48. (Previously Presented) A method according to claim 46 wherein said active matrix circuit is incorporated into an image sensor.

49. (Currently Amended) A method according to claim 46 wherein ~~said semiconductor layer comprises an amorphous semiconductor island having~~ each of said semiconductor islands comprises amorphous semiconductor and has a plane area of 1000 μm^2 or less.

50. (Currently Amended) A method according to claim 49 further comprising crystallizing said amorphous semiconductor ~~island~~.

51. (Currently Amended) A method for forming an active matrix circuit comprising a transistor, said method comprising:

forming an active layer comprising a plurality of semiconductor islands arranged in parallel to each other over a substrate;

doping a p-type impurity into ~~a semiconductor~~ said active layer by ion doping to form a source region and a drain region in said ~~semiconductor~~ active layer, said ~~semiconductor~~ active layer comprising a part to become a channel region between said source region and said drain region;

forming a gate electrode adjacent to said part to become said channel region;

activating said p-type impurity by annealing; [[and]]

forming a first interlayer insulating film comprising a silicon nitride layer and a silicon oxide layer over said ~~semiconductor~~ active layer by plasma CVD, said silicon nitride layer and said silicon oxide layer formed over said gate electrode and said ~~semiconductor~~ active layer;

forming a conductive layer comprising a titanium and an aluminum over said first interlayer insulating film;

forming a second insulating film comprising silicon oxide over said conductive layer; and

forming a pixel electrode over said second insulating film,

wherein said transistor of said active matrix circuit comprises said channel region and said gate electrode and said source region and said drain region.

52. (Previously Presented) A method according to claim 51 wherein said active matrix circuit is incorporated into a liquid crystal display.

53. (Previously Presented) A method according to claim 51 wherein said active matrix circuit is incorporated into an image sensor.

54. (Currently Amended) A method according to claim 51 wherein ~~said semiconductor layer comprises an amorphous semiconductor island having~~ each of said semiconductor islands comprises amorphous semiconductor and has a plane area of 1000 μm^2 or less.

55. (Currently Amended) A method according to claim 54 further comprising crystallizing said amorphous semiconductor ~~island~~.

56. (Currently Amended) A method for forming an active matrix circuit comprising a transistor, said method comprising:

forming an active layer comprising a plurality of semiconductor islands arranged in parallel to each other over a substrate;

doping a p-type impurity into ~~a semiconductor~~ said active layer by ion doping to form a source region and a drain region in said ~~semiconductor~~ active layer, said ~~semiconductor~~ active layer comprising a part to become a channel region between said source region and said drain region;

forming a gate electrode adjacent to said part to become said channel region;

activating said p-type impurity by annealing;

forming a first interlayer insulating film comprising a silicon nitride layer and a silicon oxide layer over said ~~semiconductor~~ active layer by plasma CVD, said silicon nitride layer and said silicon oxide layer formed over said gate electrode and said ~~semiconductor~~ active layer;

forming a conductive layer comprising a titanium and an aluminum over said first interlayer insulating film;

forming a second insulating film comprising silicon oxide over said conductive layer; and

forming a pixel electrode comprising indium tin oxide over said second insulating film,

wherein said transistor of said active matrix circuit comprises said channel region and said gate electrode and said source region and said drain region.

57. (Previously Presented) A method according to claim 56 wherein said active matrix circuit is incorporated into a liquid crystal display.

58. (Previously Presented) A method according to claim 56 wherein said active matrix circuit is incorporated into an image sensor.

59. (Currently Amended) A method according to claim 56 wherein said semiconductor layer comprises an amorphous semiconductor island having each of said semiconductor islands comprises amorphous semiconductor and has a plane area of 1000 μm^2 or less.

60. (Currently Amended) A method according to claim 59 further comprising crystallizing said amorphous semiconductor ~~island~~.